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10/736,343	12/15/2003	Rajendra K. Bera	JP920010326US1	4635

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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,343	BERA, RAJENDRA K.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-8, 10-14, 17 and 18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. According to the interm guidelines, the claims do not produce a tangible result. For example, in claim 1, the actions of "associating," "determining," and "calculating" do not produce any real world applicability. These steps merely recite "abstract ideas," Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759.

For more information on the interm guidelines, visit http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. As per claim 13:

Claim 13 states that the values of p in S are bit patterns in bit vectors. However, claim 11 states that S is a **product** of the p(I) associated with each I entry. The examiner fails to see how the method of claim 13 can be completed by multiplying the bit patterns of p to get S. It is the understanding of the examiner that each p(I) for each value I is simply joined to make a bit vector S. For the purposes of this action, the words "the product of" in claim 11 will be replaced with "based on" to correct the problem in claim 13.

6. As per claim 15:

The last word of 15 is "and" which is not followed by another limitation. The "and" should be removed or another limitation should be added.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 8-11 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by "Non-linear array data dependence test" by Huang and Yang.

9. As per claim 1:

A method for detecting cross-iteration dependencies between variables in a loop of a computer program, the method comprising the steps of:

associating unique values with each of the values of indirect loop index variables of the loop (Section 3) (Each possible value of the function that is used in the loop is marked with the iteration that the access will be made. This is a unique value because the assumption that the function is either monotonically increasing or decreasing is made (i.e. cos(x) can not be tested));

calculating for each iteration of the loop an indirectly indexed access pattern based upon the associated unique values (Section 3) (array T); and

determining whether cross-iteration dependencies exist between any two iterations of the loop based upon the indirectly indexed access pattern of the two iterations (Section 3).

10. As per claim 2:

The method as claimed in claim 1, wherein the unique values associated with each of the values of the indirect loop index variables of the loop are different binary bit patterns of a bit vector (Section 3) (Each of the unique values will inherently be different binary patterns since no two binary numbers are the same. Huang's array is a bit vector because arrays are stored sequentially.).

11. As per claim 8:

The method as claimed in claim 1, further comprising the step of grouping iterations in a wave for execution in a common time period such that no cross-iteration dependencies exist between any of the grouped iterations of the wave (Section 3).

12. As per claim 9:

The method as claimed in claim 8, further comprising the step of executing each of said waves in a prescribed sequence, and executing each of said iterations in each of said waves in parallel with each other (Section 3, last paragraph, particularly last sentence).

13. As per claim 10:

A method for assisting in scheduling parallel computation of instructions in a loop of a computer program, the method comprising the steps of:

determining, for a loop, active array variables, and direct and indirect loop index variables (Sections 1 and 3) (Section 1 refers to array variables with indirect loop index variables (direct is inherent), while section 3 states that all potential dependencies are checked.);

determining, for each iteration of the loop, values of the indirect loop index variables (Section 3);

associating a unique value with each of values of the indirect loop index variables (Section 3);

calculating an indirectly indexed access pattern for each iteration of the loop (Section 3); and

determining whether cross-iteration dependencies exist between any two iterations of the loop based upon the indirectly indexed access patterns of the two iterations (Section 3).

14. As per claim 11:

A method for detecting cross-iteration dependencies between variables in a loop of a computer program, the method comprising the steps of:

determining, for a loop, Boolean conditions embedded in the loop (Figure 2) (While Huang does not explicitly talk about dealing with the conditionals in the loop, such is inherent since the method deals with embedded loops);

determining possible decision paths an iteration is allowed to take in the loop body in the presence of Boolean conditions (Inherent);

determining a first set $V=\{v_1, v_2, \ldots v_n\}$ of active array variables of the loop, and a second set $I=\{i_1, i_2, \ldots i_r\}$ of indirect loop index variables that appear with the active array variables of said first set in the loop (Sections 1 and 3);

determining, for each decision path λ in the set of possible decision paths in the loop, the set V_λ of active array variables associated with the path, and the set I_λ of indirect loop index variables that appear with the active array variables V_λ (Figure 2 and Section 3) (Inherent);

determining the range $[N_1, N_2]$ of the direct loop index i of the loop, and the maximal range $[M_1, M_2]$ of the set of indirect loop index variables $i_1, i_2, \ldots i_r$ of the loop (Section 3);

associating, for each value I of the indirect loop index variables in the range [M_1, M. $_2$], a unique value p(I) with each value I of the indirect loop index variables in the range [M_1, M_2] (Section 3);

determining, for each pair (i, λ) of a value of the direct loop index i and a decision path λ in the set of all possible decision paths in the loop, the value of S_λ (i) where S_λ (i) is based on the unique values p(I) associated with each value I of the indirect loop index variables in the range [M_1, M_2] (Section 3); and

determining, for any pair S_α (i) and S_β (j), whether the values of S_α (i) and S_β (j) indicate that cross-iteration dependencies exist between iterations i and j (Section 3).

15. As per claim 14:

The method as claimed in claim 11, further comprising the step of:

grouping loop iterations in waves such that any two iterations i and j of a particular wave have no cross-dependencies (Section 3).

16. As per claim 15:

The method as claimed in claim 14, further comprising the step of: executing the waves in which loop iterations are grouped in a predetermined sequence such that the wave having the lowest value of the direct loop index i is executed first and completely, followed by the wave with the next lowest value of i, and so on for successive values of i (Section 3).

17. As per claim 16:

The method as claimed in claim 14, further comprising the step of: executing the iteration in each wave in parallel using multiple computing processors (Section 3, last

paragraph, particularly last sentence) (Huang states that the waves are executed in parallel. It is not explicitly stated that this is done on separate processors, however, Huang states that his method is applicable to the HP SPP2000 (Abstract), which has 64 processors. Therefore, it is inherent that the waves are executed in parallel on other processors).

18. As per claim 17:

A computer program product for detecting cross-iteration dependencies between variables in a loop of a computer program, the computer program product comprising computer software stored on a computer-readable medium for performing the steps of:

associating unique values with each of the values of indirect loop index variables of the loop (Section 3);

calculating for each iteration of the loop an indirectly indexed access pattern based upon the associated unique values (Section 3); and

determining whether cross-iteration dependencies exist between any two iterations of the loop based upon the indirectly indexed access pattern of the two iterations (Section 3).

While Huang does not explicitly disclose a computer readable medium, such is inherent to be able to execute the method described by Huang in a computer system.

19. As per claim 18:

A computer system for detecting cross-iteration dependencies between variables in a loop of a computer program, the computer system executing computer software stored on a computer-readable medium for performing the steps of:

associating unique values with each of the values of indirect loop index variables of the loop (Section 3);

calculating for each iteration of the loop an indirectly indexed access pattern based upon the associated unique values (Section 3); and

determining whether cross-iteration dependencies exist between any two iterations of the loop based upon the indirectly indexed access pattern of the two iterations (Section 3).

While Huang does not explicitly disclose the system in which his method runs on, such is inherent.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 3, 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Non-linear array data dependence test" by Huang and Yang as applied to claim 2 in view of Structured Computer Organization by Tanenbaum.

22. Huang teaches claim 2 for the reasons stated above.

23. As per claim 3:

Huang does not teach the method as claimed in claim 2, wherein the indirectly indexed access pattern for an iteration is calculated by forming the logical AND of the

unique bit patterns associated with each of the values of the indirect loop index variables of the loop for that iteration.

Huang teaches that when T(g(i)) is checked, if it != 0 then a dependence is present between f and g at array access q.

Huang states that his method is used in a paralleling compiler (Huang: Section 3). However, Huang teaches his method being used in loops with indirect indexing (Huang: Figure 1). One of ordinary skill in the pertinent art would have recognized that program profiling would have to be done to be able to perform the method. Even then, correct scheduling would not be guaranteed (e.g. a negative number used for an N would produce different dependencies). Therefore, for Huang's method to be truly effective, it must be used at runtime.

Tanenbaum teaches that hardware and software are logically equivalent and that any operation performed by software can be implemented in hardware (Tanenbaum 11). Further, Tanenbaum specifically states that indirect indexing of arrays is now better handled by hardware (Tanenbaum 12).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Huang in hardware would provide the benefit of eliminating profiling and providing guaranteed correct scheduling.

In Huang's method, T(g(i)) is checked for != 0. In a compiler, this is a simple one-line action. However, when implementing Huang in hardware as provided above, this requires a 32-bit comparator or a 32-bit input OR gate / cascading OR gates. This also has to be done within the decode/dispatch stage so the use of the execution units

cannot be used without further circuitry and taking up valuable resources. One of ordinary skill in the pertinent art would have recognized that this is not efficient. The most viable solution is to include a 33rd bit for each entry in the T array, which would be signified as the NEZ bit (not equal to zero bit). Therefore, rather than checking all 32 bits for being non-zero, the single bit would instead be checked. This of course would be accomplished by a 1 input AND gate as addressed by the limitations of the claim.

Therefore, one of ordinary skill in the pertinent art at the time of the applicant's invention would have recognized that using a 1 input AND gate to test the unique bit patterns associated with each of the values of the indirect loop index variables of the loop of that iteration would provide simpler, more efficient logic.

24. As per claim 4:

The method as claimed in claim 3, wherein the existence of cross-iteration dependencies is determined by determining whether the indirectly indexed access pattern for the two iterations have any common bit positions that share a value of one (Section 3) (Using the method outlined above, this would remain true.).

25. As per claim 13:

The method as claimed in claim 11, wherein the unique values p(l) are different bit patterns in a bit vector, and the values of S_α (i) and S_β (j) indicate that no cross-iteration dependencies exist between iterations i and j if S_α (i) and S_β (j) share any common bits that are set to 1 when i != j (Section 3) (motivation to use bits set to 1 instead of != 0 is provided above).

26. Claims 5-7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang as applied to claims 1 above, and in view of Algebraic Aspects of Cryptography by Koblitz and "A New Access Control Method Using Prime Factorisation" by Hwang.

27. Huang teaches claims 1 and 11 for the reasons stated above.

28. As per claim 5:

Huang does not teach the method as claimed in claim 1, wherein the unique values associated with each of the values of the indirect loop index variables of the loop are different prime numbers.

Using prime factorization in a key and lock method is a well-known method in the art of cryptography (Hwang 2.1). In this method, each user is assigned a unique prime key, which is then factored into the lock. When the user attempts to access the host, the greatest common divisor (gcd) between the key and the lock is determined. If gcd = key, then the access is granted. The runtime of this method is O(ln(a)*ln(b)), where au + bv = d and a > b > 0 (Koblitz 28).

One of ordinary skill in the art will recognize that this is faster than a search method with a runtime of O(n) wherein n is the total number of entries.

One of ordinary skill in the art will also recognize that this method is also applicable to Huang since the value of T(q) is only used for determining the wavefront and is inconsequential to determining if there is a match. Therefore each value of T != 0 would instead be given a prime number tag. Depending on whether the access is from f or g, the value will be multiplied to a total number S1 or S2. To determine a

dependence between S1 and S2, the gcd would be found between them. If the gcd > 1, then a dependence exists.

29. As per claim 6:

The method as claimed in claim 5, wherein the indirectly indexed access pattern for an iteration is calculated by forming the product of the unique prime numbers associated with each of the values of the indirect loop index variables of the loop for that iteration (Using the method described above, this would be true).

30. As per claim 7:

The method as claimed in claim 6, wherein the existence of cross-iteration dependencies is determined by determining whether a greatest common divisor between the two indirectly indexed access patterns for the two corresponding iterations is greater than one (Using the method described above, this would be true).

31. As per claim 12:

The method as claimed in claim 11, wherein the unique values p(l) are different prime numbers and the values of S_α (i) and S_β (j) indicate that no cross-iteration dependencies exist between iterations i and j if the greatest common divisor of S_α (i) and S_β (j) is 1 when i != j (Using the method described above, this would be true).

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakahira et al. (US Patent 5,842,022) addresses indirect indexing.

Blume et al. "The Range Test: A Dependence Test for Symbolic, Non-linear Expressions" deals with an indirect indexing test.

Huang et al. "A Practical run-time technique for exploiting loop-level parallelism" teaches runtime dependency checking.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
Art Unit 2183

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